EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S82	2131	@ad<"20031128" And ((Ocok\$3 "clk" "ck" delay buffer driver) with (budget\$3 allocat\$4 distribut\$3 assign\$5 allot \$5 tree\$3) same (schematic netlist\$3 ((net gate) near2 list\$3) (logic \$3 near2 (phase stage)) rtl (rtl (register near3 (transfer\$3) near3 (level \$3 language code program algorithm description representation)) hdl verilog (hardware near3 (language code program algorithm description representation) near3 (language code program algorithm)))))	US PGPUB; USPAT; USOCR; EPC, JPO; DEFM/ENT; IBM_TDB	OR	ON	2009/04/26
S83	123	@ad-"20031128" And ((Ocok\$3" clk" "ok" oleiay buffer driver) with (budget\$3 allocat\$4 distribut\$3 assign\$5 allot \$5 tree\$3) same (schematic netlist\$3 ((net gate) near2 list\$3) (logic \$3 near2 (phase stage)) rtl (rtl (register near3 (transfer\$3) near3 (level \$3 language code program algorithm description representation)) hdl verilog (hardware near3 (description representation) near3 (language code program algorithm)))) and (rtl (register near3 (transfer\$3) near3 (level\$3 language code program algorithm description representation)) hdl verilog (hardware near3 (description representation)) hdl verilog (hardware near3 (description representation)) near3 (language code program algorithm description representation)) near3 (language code program (language code program algorithm)) near3 (language code program algorithm)	US-PGFUE; USPAT; USOCR; EPC, JPO; DEFM/BNT; IBM_TDB	OR	ON	2009/04/26

S84	162	@ad-"20031128" And ((Clock\$3" clk" "ck" oldely buffer driver) with (budget\$3 allocat\$4 distribut\$3 assign\$5 allot \$5 tree\$3) same (schematic netlist\$3 ((net gate) near2 (phase stage)) rtl (rtl (register near3 (transfer\$3) near3 (level \$3 language code program algorithm description representation)) hdl verilog (hardware near3 (description representation) near3 (language code program algorithm)))) and 716/6.cols.	US-PAPUE; US-PAP	OR .	ON	2009/04/26 18:04
S85	110	@ad<"20031128" And ((Clock\$3 "clk" "ck" delay buffer driver) with (budget\$3 allocat\$4 distribut\$3 assign\$5 allot \$5 tree\$3) same (schematic netlist\$3 ((net gate) near2 list\$3) (logic \$3 near2 (phase stage)) rtl (rtl (register near3 (level \$3 language code program algorithm description representation)) hdl verilog (hardware near3 (description representation)) near3 (language code program algorithm))))) and 716/6.cods. and (layout (lay adj out\$4))	US-PCPUB; USPAT; USOCR; EPC; JPC; DETWIENT; IBM_TDB	OR	ON	2009/04/26 18:06

S88	431	@ad<"20031128" And (((timing time clock\$3) near5 (analy\$7 verif\$7 test\$3 validat\$4 check\$4 optim\$7 correct\$3 fix\$3) or sta) with (((circuit logic\$3) near2 (design) (logic\$3 near2 (stage design phase)) netlist ((net gate) near2 (stage design phase)) netlist ((net gate) near2 (stage design phase)) near3 (transfer\$3) near3 (tevel\$3 language code program algorithm description representation)) hdl verilog (hardware near3 (language code program algorithm)))) And (((timing time clock\$3) near5 (analy\$7 verif\$7 test\$3 validat\$4 check\$4 optim\$7 correct\$3 fix\$3) or sta) with layout\$3}	US-PGPUB; USPAT; USOCR; EPC), JPO; DEFWENT; IBM_TDB	OR	ON	2009/04/26 18:21
S89	431	@ad<"20031128" And (((timing time clock\$3) near5 (analy\$7 verif\$7 test\$3 validat\$4 check\$4 optim\$7 correct\$3 fix\$3) or sta) with (((circuit logic\$3) near2 (etsage design phase) netlist ((net gate circuit) near2 list\$3) (rtl (register near3 (transfer\$3) near2 (level\$3 language code program algorithm description representation)) hdl verilog (hardware near3 (description representation)) near3 (language code program algorithm) (clest) (language code program algorithm))))) And (((timing time clock\$3) near5 (analy\$7 verif\$7 test\$3 validat\$4 check\$4 optim\$7 correct\$3 fix\$3) or sta) with layout\$3)	US-PGPUB; USPAT; USOOR; EPC, JPC; DEFWENT; IBM_TDB	ÖR	ON	2009/04/26 18:22

\$90	340	(@ad<"20031128" And (((timing time clock\$3) near5 (analy\$7 verif\$7 test\$3 validat\$4 check\$4 optim\$7 correct\$3 fix\$3) or sta) with (((circuil logic\$3) near2 (etage design phase)) netlist ((net gate circuil) near2 (isis\$3) (rll (register near3 (transfer\$3) near3 (level\$3 language code program algorithm description representation)) hdl verilog (hardware near3 (language code program algorithm)))) And (((timing time clock\$3) near5 (analy\$7 verif\$7 test\$3 validat\$4 check\$4 optim\$7 correct\$3 fix\$3) or sta) with layout\$3 and ("700" "703" "716" "717").(description") "71	US POPUB; USPAT; USOOR; EPC, JPO; DEFIMENT; IBM_TDB	OR	ON	2009/04/26 18:23
S91	487	@ad<"20031128" And (((timing time clock\$3) near5 (analy\$7 verif\$7 test\$3 validat\$4 check\$4 optim\$7 correct\$3 fix\$3 satist\$7 meet\$3 met) or sta) with (((circuit logic \$3) near2 (design) (logic \$3 near2 (stage design phase)) netlist ((pre prior before) adj2 layout) ((net gate circuit) near2 list\$3) (rtl (register near3 (transfer\$3) near3 (level \$3 language code program algorithm description representation) hdl verilog (hardware near3 (description representation) near3 (language code program algorithm))) And (((timing time clock\$3) near5 (analy\$7 verif\$7 test\$3 validat\$4 check\$4 optim\$7 correct\$3 fix\$3	US PGPUB; USPAT; USGOR; EPC, JPC; DERWENT; IBM_TDB	OR	ON	2009/04/26 18:31

		satisf\$7 meet met) or sta) with layout\$3)				
S92	382	S91 and ("716" "703" "700" "717").clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 18:33
S93	12	(US-200500114818-\$ or US-2005009162-\$ or US-20040230933-\$ or US-20040107408-\$ or US-20040015803-\$ or US-200300188268-\$ or US-2003008842-\$ or US-20030023938-\$ or US-20030023938-\$ or US-20020188918-\$ or US-2002018-\$ or US-2002018-\$ or US-2002018-\$	US-PGPUB	OR	ON	2009/04/26 19:38
S94	7	S93 and (allocat\$4 schedul\$3 distribut\$4 ds tree\$3) and (skew\$3 slack \$3)	US-PGPUB	OR	ON	2009/04/26 19:40
S101	21	(US-20050050497-\$ or US-20030177455-\$ or US-20030177455-\$ or US-20050102643-\$ or US-20040107408-\$ or US-200400176767-\$ or US-20040040753-\$ or US-20050114818-\$ or US-20050114818-\$ or US-2005001621-\$ or US-200400230933-\$ or US-200400288662-\$ or US-20030088862-\$ or US-20030088842-\$ or US-20030061585-\$ or US-20030162086-\$), idi. or (US-6473890-\$ or US-6536024-\$ or US-5974245-\$ or US-5933336-\$ o, idi.	US-POPUB; USPAT	OR	ON	2009/04/26 23:06

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